I N S T R U C T I O N M A N U A L

MODEL 82AD-01

IEEE 488-1975 BUS INTERFACE OPTION

p o c

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLES

FIGURES

SECTION I

INTRODUCTION

1.1 SCOPE OF MANUAL

1.2 This handbook provides descriptive data, operating instructions, theory of operation, maintenance instructions, and a parts list for the Model 82AD-01 IEEE 488-1975 Bus Interface Option. (See Figure 1-1.) The 82AD-01 is manufactured by Boonton Electronics Corporation, Parsippany, New Jersey.

1.3 PURPOSE AND USE OF EQUIPMENT

1.4 The Model 82AD-01 is a microprocessor controlled interface adapter which generates control signals for, and reads, panel, panel meter, and status data from the 82AD circuits and generates IEEE 488 Bus compatible signals. The interface is implemented on two circuit boards, one which plugs into the 82AD main frame, and one which is mounted on the 82AD rear panel. Among the operating features are:

a. Automatic range readout via an inserted decimal point in the digital panel meter data string.

b. Selectable output format to suppress unwanted data.

c. Binary programming format for single string programming of front panel controls.

d. Data output format control in the "TALK ONLY" mode, via the address selection switch.

1.5 The features described in the preceding paragraphs, together with those described in Table 1-1, make the 82AD-01 a flexible interface for automatic communications and metrology test systems.

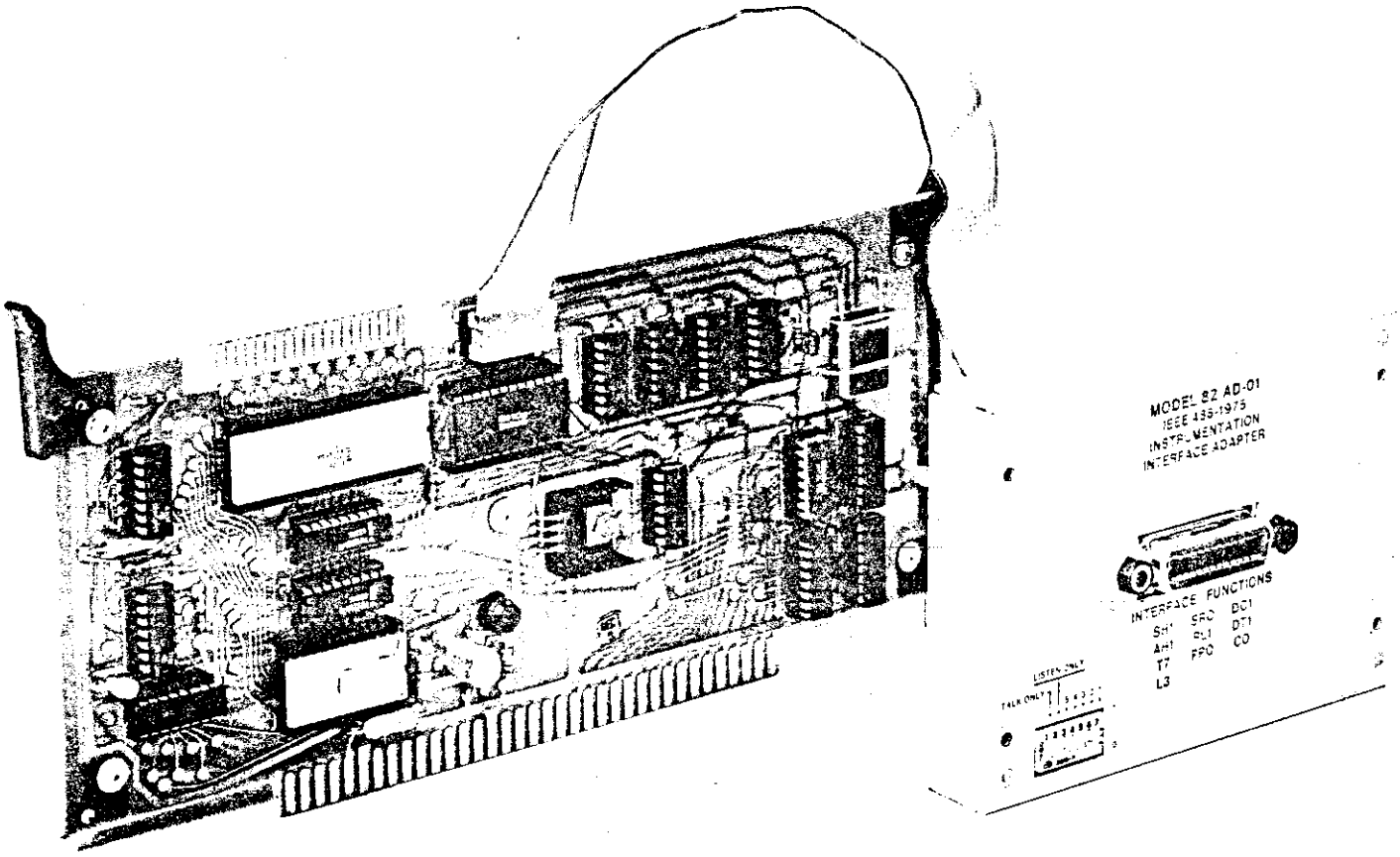


Figure 1-1. Model 82AD-01 IEEE 488-1975 Bus Interface Option

1.6 PERFORMANCE SPECIFICATIONS

1.7 Pertinent performance specifications of the Model 82AD-01 are listed in Table 1-1.

TABLE 1-1.

Interface Function:	SH1, AH1, T7, L3, SR0, RL1, PP0, DC1, DT1, C0
Address Selection:	7 position "dip" switch selects decimal address or TALK or LISTEN only modes. Address switch positions 1 - 3 control output data format in TALK only mode.
Bus Connector:	All data and bus management lines are compatible with IEEE-488-1975 specifications.
Power Requirements:	Internally powered from 82AD mainframe.
Operating Temperature:	0 - 55°C

SECTION II

OPERATION

2.1 GENERAL

2.2 This section contains instructions for the installation and operation of the Model 82AD-01. It is recommended that the instrument operator be familiar with the material in this section before attempting to operate the equipment; otherwise the full capability of the interface may not be realized in use.

2.3 INSTALLATION

NOTE: If the option is already installed in a new 82AD, proceed to Paragraph 2.6.

2.4 Unpacking. The Model 82AD-01 is shipped complete and ready for installation upon receipt. Unpack the interface assembly and processor board from the shipping container and inspect them for damage that may have occurred during shipment. Check that all IC's are seated in their sockets and that the address switch operates properly.

NOTE: Save the packing material and container for possible use in reshipment of the equipment.

2.5 Refer to the 82AD Instruction Manual for instructions on removing the instrument cover and proceed as follows:

a. Remove the trim plate on the 82AD rear panel by removing four No. 4-40 x 1/4" binder head screws.

b. Insert the 16-pin ribbon connector into the socket provided on the interface board assembly. See Figure 2-1.

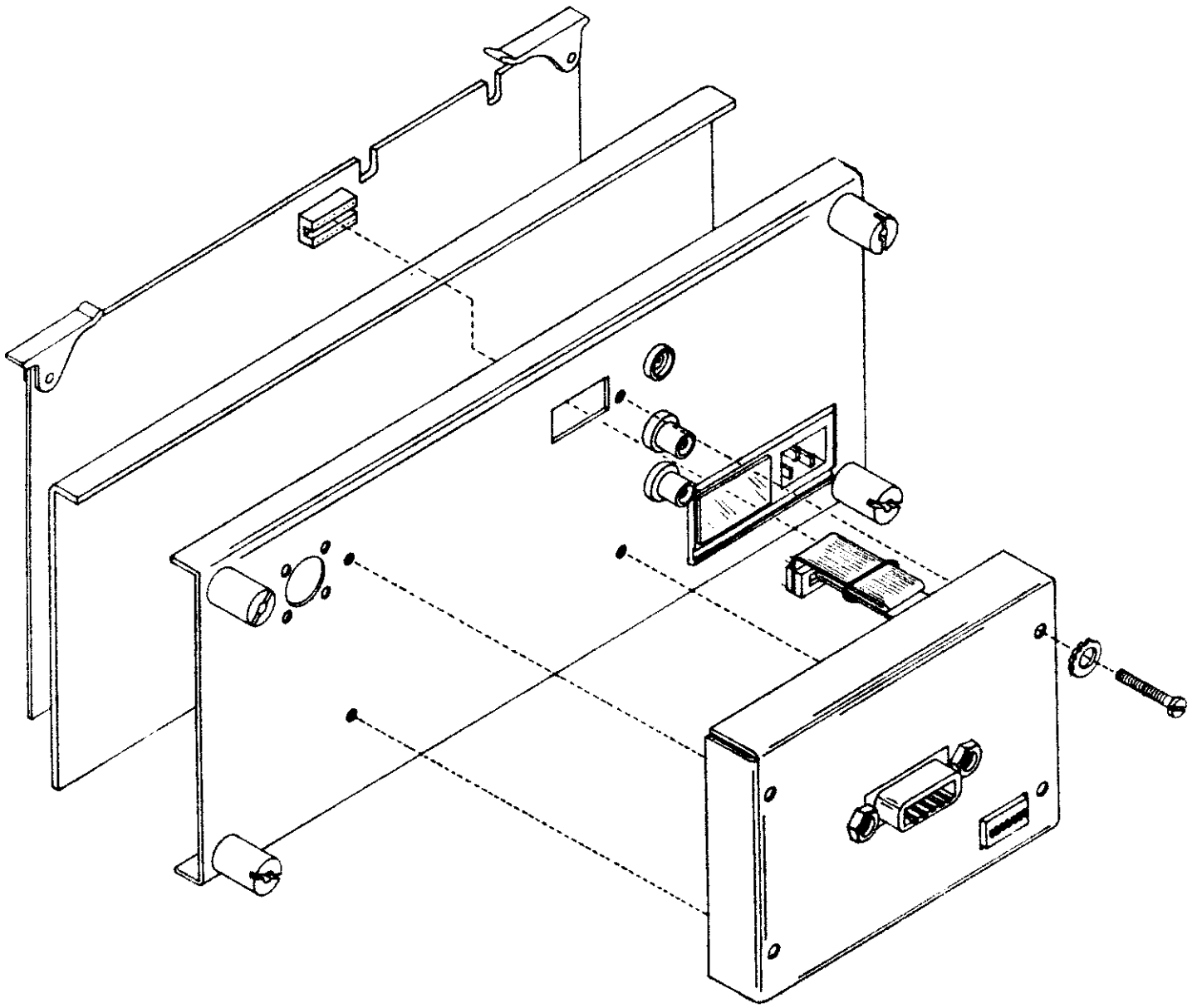


Figure 2-1. Option -01 Installation

c. Feed the flat cable through the cutout provided on the 82AD rear panel and assemble the interface assembly to the 82AD using the four No. 4-40 x 1-1/4" binder head screws provided.

CAUTION: The processor board is inserted into the 82AD frame with the components facing toward the rear panel of the instrument.

d. Insert the processor board into the rear card guides (observing the above precaution) and seat the board in the 72 pin connector.

e. Insert the 16-pin flat cable connector into the socket provided on the processor board.

f. Clip the flat cable folds with the clip provided.

2.6 Cable Connections. The only cable connection required is the IEEE-488 Bus interface cable supplied with each 82AD-01.

NOTE: If the 82AD-01 is installed in a new 82AD, refer to the 82AD manual for preliminary checks before proceeding.

2.7 OPERATION. The Model 82AD Modulation Meter may be remotely controlled via IEEE Std. 488-1975 Digital Interface Compatible Instrumentation. The capability of the 82AD when connected to the Interface Bus is specified in Table 2-1. These interface functions are also reproduced above the interface connector on the rear panel of the 82AD.

Table 2-1

INTERFACE FUNCTIONS

SH1	Source handshake capability
AH1	Acceptor handshake capability
T7	Talker (basic talker, no serial poll talk only mode, unaddressed to talk if addressed to listen)

Table 2-1. (Continued)

INTERFACE FUNCTIONS

L3	Listener (basic listener, listen only mode, unaddress to listen when addressed to talk)
SR0	No service request capability
RL1	Remote/Local capability
PP0	No parallel poll capability
DC1	Device clear capability
DT1	Device trigger capability
C0	No controller capability

2.8 ADDRESS SELECTION. The talk and listen addresses of the 82AD are selected by the address selector switch (Figure 2-2) located on the rear panel. This switch is a seven position "DIP" switch with positions marked "1" through "5" as the address code and positions 6 and 7 for talk or listen only selection. Table 2-2 lists the available address codes and the corresponding switch settings.

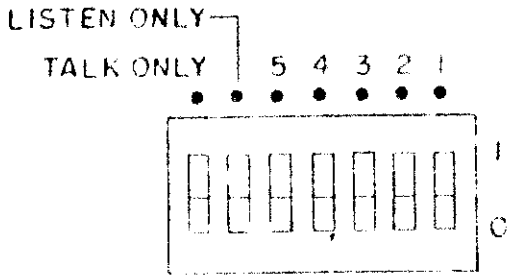


Figure 2-2

Table 2-2

ADDRESS SELECTION

ASCII Code Character		Address Switches					
Listen	Talk	A5	A4	A3	A2	A1	5-bit Decimal Code
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	0	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
-	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
ø	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26

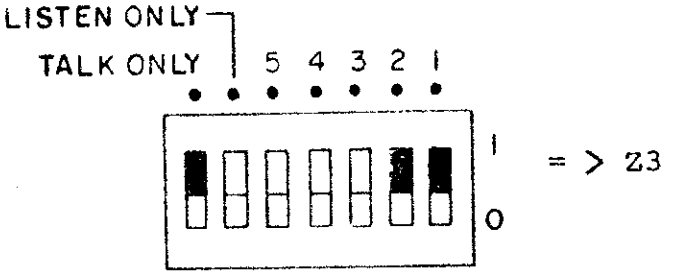
Table 2-2. (Continued)

ADDRESS SELECTION

ASCII Code Character		Address Switches					
Listen	Talk	A5	A4	A3	A2	A1	5-bit Decimal Code
;	[	1	1	0	1	1	27
<	\	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

2.9 TALK ONLY. The 82AD is placed in the talk only mode by setting the TALK ONLY switch, located on the rear panel, to the "1" position. In this mode the 82AD will continuously output data in the format defined in Table 2-5 by using Address Switch positions 1 - 3 to select BCD equivalents of Z1 - Z3.

For example:



2.10 LISTEN ONLY. The 82AD is placed in the listen only mode by setting the LISTEN ONLY switch, located on the rear panel, to the "1" position. In this mode the 82AD can be used under remote front panel control using the programming codes detailed in Paragraph 2.11.

2.11 PROGRAM CODES. All front panel controls except the power switches and the "Level" control are programmable via the Interface Bus. The program codes for each switch are listed in Table 2-3.

Table 2-3

PROGRAM CODES

Switch	Position	Program Code
Tuning	Auto	T1
	EXT	T2
High-Pass	10	H1
	30	H2
	300	H3
	3000	H4
Low-pass	3 kHz	L1
	15 kHz	L2
	120 kHz	L3
	200 kHz	L4
De-emphasis	50 µs	D1
	75 µs	D2
	750 µs	D3
	6 dB/OCT	D4
Peak	+	P1
	-	P2
	$\frac{PK - PK}{2}$	P3

Table 2-3. (Continued)

PROGRAM CODES

Switch	Position	Program Code
Range	300	R1
	100	R2
	10	R3
Function	kHz	F1
	%AM	F2
	Level	F3

2.12 PROGRAMMING. The 82AD is programmed by data messages sent by the system controller. These messages are composed of the address command and the program information. The address command consists of the talk address of the controller and the listen address of the 82AD. The program information consists of the codes of the 82AD controls to be programmed. Syntax for the address command is a function of the system controller, and for the 82AD according to the codes listed above.

Example No. 1 (using a Tektronix 4501 controller): The following program line will set the 82AD to Auto tuning, 30 Hz high-pass, 15 kHz low-pass, $\frac{PK-PK}{2}$, 100 range, and kHz dev.

```
190                .....
200                PRINT @ 18:  "T1H2L2P3R2F1"
210                .....
```

18 is the decimal address of the 82AD and the string within quotation marks is the data transmitted.

Any or all of the programming codes may be transmitted in any sequence in one data string.

In addition the 82AD may be programmed by a Fixed Format Alpha-numeric string.

$$B\ N_1N_2N_3N_4N_5N_6$$

The "B" prefix tells the 82AD to expect a six digit string. Control settings are tabulated in Table 2-4.

Example No. 2: For example,

```
190                 .....
200                 PRINT @ 18:  "B112321"
210                 .....
```

also causes the 82AD to be set to Auto tuning, 30 Hz high-pass, 15 kHz low-pass, $\frac{PK-PK}{2}$, 100 range, and kHz dev.

Table 2-4

Digit	Control	Setting
N_1	Tuning	1, Auto
		2, External
N_2	High-pass	1, 10 Hz
		2, 30 Hz
		3, 300 Hz
		4, 3000 Hz
N_3	Low-pass/De-emphasis	1, 3 kHz Low-pass
		2, 15 kHz Low-pass
		3, 120 kHz Low-pass
		4, 200 kHz Low-pass

Table 2-4. (Continued)

Digit	Control	Setting
N_3 (Continued)	Low-pass/De-emphasis	5, 50 µs De-emphasis
		6, 75 µs De-emphasis
		7, 750 µs De-emphasis
		8, 6 dB/OCT De-emphasis
N_4	Peak	1, +
		2, -
		3, $\frac{PK-PK}{2}$
N_5	Range	1, 300
		2, 100
		3, 10
N_6	Function	1, kHz
		2, % AM
		3, Level

2.13 DATA OUTPUT FORMATS. Data output format for the 82AD is under control of the system controller.

The 82AD is first addressed to listen and a control code is transmitted. This control code is interpreted by the 82AD according to Table 2-5.

Table 2-5

Control Code	
Z_1	Status, control settings, DPM data<CR><LF>
Z_2	Status, control settings<CR><LF>

Table 2-5. (Continued)

Control Code

Z_3	Status, DPM data<CR><LF>
Z_4	Status<CR><LF>
Z_5	Control settings, DPM data<CR><LF>
Z_6	Control settings<CR><LF>
Z_7	DPM data<CR><LF>

If no control is transmitted the 82AD assumes the "Z_3" talk format. For example:

```
190       .....
200       PRINT @ 18:  "Z5"
210       .....
```

programs the 82AD to output control settings, ASCII comma, DPM data, carriage return and line feet.

Output data format will continue according to the current control code until the 82AD is again addressed to listen and a new control code is transmitted.

2.14 STATUS FORMAT. Instrument status is transmitted as a number from 0 to 7. The transmitted number may be interpreted as follows:

	Level Error	Overranged DPM	Lock
0	NO	NO	NO
1	NO	NO	YES*
2	NO	YES	NO

Typical output:

```
?H2L2P3R2F1 RETURN

   STATUS          PANEL          DPM

     1             122321         83.5

?
```

Program No. 2:

```
 90                B = 0
100                PRINT @ 18:  "Z6"                Set output format
105                WBYTE @ 18,1:                    Go to local
110                INPUT @ 18:  A                   Read data
120                IF A = 111111 THEN 170           Test data
130                If A = B THEN 110                Test data
140                B = A
150                PRINT B
160                GO TO 110
170                END
```

Sample program two causes panel settings to be read continuously and displayed whenever a change occurs.

Program No. 3:

```
100                PRINT "DEVIATION TRACKING:"      )
110                PRINT                            ) Heading
120                PRINT "TO BEGIN TEST - HIT RETURN" )
130                INPUT A$
140                PRINT @ 18:  "T1H2L2P3R2F1Z1"    Set controls
```

Program No. 3 (Continued):

```
150   FOR I = 1 TO 5                          )
160   PRINT "SET FREQUENCY - HIT RETURN"      )
170   INPUT B$                                )
180   INPUT @ 18:  A, B, C                    )
185   IF A = 1 THEN 190                       )   Read five deviations
187   GO TO 180                               )
190   D(I) = C                                )
200   NEXT I                                  )
210   F = 0
215   E = D(I)
217   G = E
220   FOR I = 1 TO 5
230   IF D(I)< = E THEN 260
240   E = D(I)                                Maximum deviation
250   GO TO 280
260   IF D(I) = > G THEN 280
270   G = D(I)                                Minimum deviation
280   F = F + D(I)                            Total deviation
290   NEXT I
300   F = F/5                                 Mean deviation
310   H = (E - G)/F * 100                     Deviation error
320   PRINT "MEAN DEVIATION", "PEAK-PEAK
        ERROR"
330   PRINT F, H
340   END
```

Sample Program 3 inputs deviation readings at five RF frequencies and computes the mean deviation and the peak-peak error in percent.

SECTION III

THEORY OF OPERATION

3.1 GENERAL

3.2 The 82AD-01 is a microprocessor driven data interface which converts IEEE 488 Bus Compatible signals into control codes which operate the 82AD internal control bus. In addition the interface converts 82AD panel, panel meter, and status signals to compatible signals for use on the Bus.

3.3 All data transfers are handled by source and acceptor handshake protocol as defined by IEEE-488-1975.

3.4 SIMPLIFIED BLOCK DIAGRAM. Figure 3-1 presents the simplified block diagram of the 82AD-01.

3.5 GENERAL. For purposes of this discussion the logic circuits of the Model 82AD-01 may be grouped by function as follows: clock and timing circuits, CPU and memory circuits, and serial interface circuits.

3.6 CLOCK AND TIMING CIRCUITS. The CPU and shift register clocks are generated by the clock and timing circuits. Timing is controlled by a 2.5 MHz crystal controlled oscillator which is divided and processed to provide signals necessary for proper CPU and shift register operation.

3.7 CPU AND MEMORY CIRCUITS. Data transfers are controlled by a Z-80 Central Processor in conjunction with 1024 bytes of Read-Only memory and 256 bytes of Random-Access memory.

3.8 SERIAL INTERFACE CIRCUITS. All IEEE 488 Bus, 82AD control bus, 82AD Status and panel meter signals are converted to serial form for transmission by the Z-80 CPU. This permits simple interconnect between the processor and interface circuit boards.

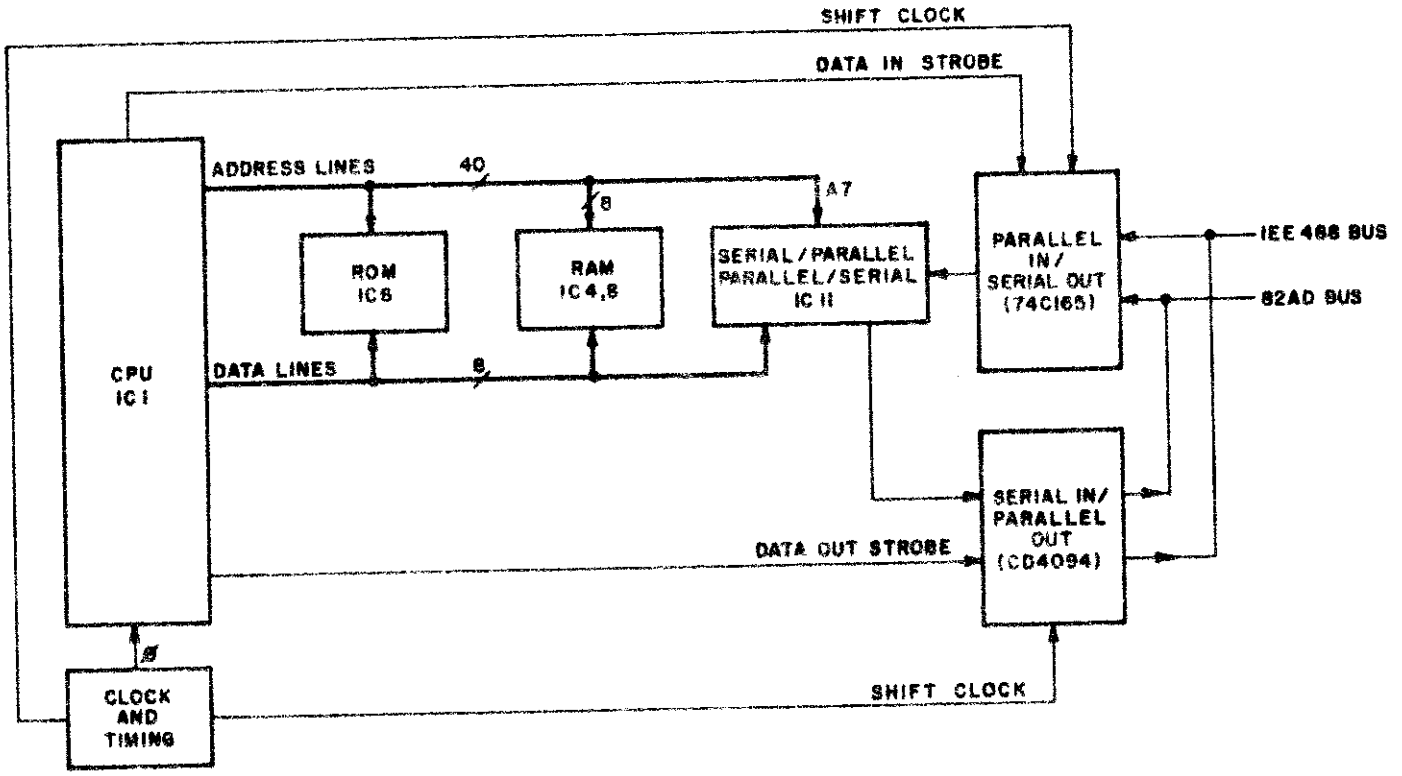


Figure 3-1. Simplified Block Diagram

3.9 DETAILED THEORY OF OPERATION, CLOCK AND TIMING CIRCUITS. See Figures 3-2 and 6-1.

3.10 Crystal Y1 and IC9e and f are connected to form a 2.5 MHz crystal oscillator. This signal is buffered by IC9c and d and divided by two in IC12 to provide a symmetrical clock waveform required by the microprocessor.

3.11 IC5b and c, IC7, and IC12 generate the shift clock signals required by the serial input and output ports. Shift signals are initiated when a software routine causes address line A7 and I/O request line $\overline{\text{IORQ}}$ to be set true. This clears counter IC7 and flip-flop IC12. When A7 or $\overline{\text{IORQ}}$ changes state the flip-flop and counter are enabled and counting begins. Counting continues until the "D" output of IC7 becomes true, terminating the count sequence. Since IC7 counts on the negative going edge of IC12's "Q" output, exactly eight clock shift pulses are generated before the sequence terminates. These signals shift 8-bit data bytes into or out of IC11.

3.12 DETAILED THEORY OF OPERATION, CPU AND MEMORY CIRCUITS. See Figures 3-3 and 6-1.

3.13 All of the data manipulation and IEEE-488 Bus management is controlled by the Z-80 CPU IC1 in conjunction with a 1024 byte micro-program stored in Read-Only memory chip IC6.

3.14 Power on reset is provided by R1, C1, and CR1. When power is applied C1 charges slowly through R1. This holds the CPU reset line "low" until the power supplies are at proper levels. A software loop holds the processor in an idle state until a handshake sequence is initiated via the IEEE-488 Bus. As a part of power on housekeeping, the random access memory (IC4 and IC8) is cleared and proper memory pointers are established.

3.15 Program flow and data transfers are controlled by micro-code stored in IC6. Random access memory is used for temporary storage of panel settings and DPM data prior to code conversion and transmission to the serial interface circuits.

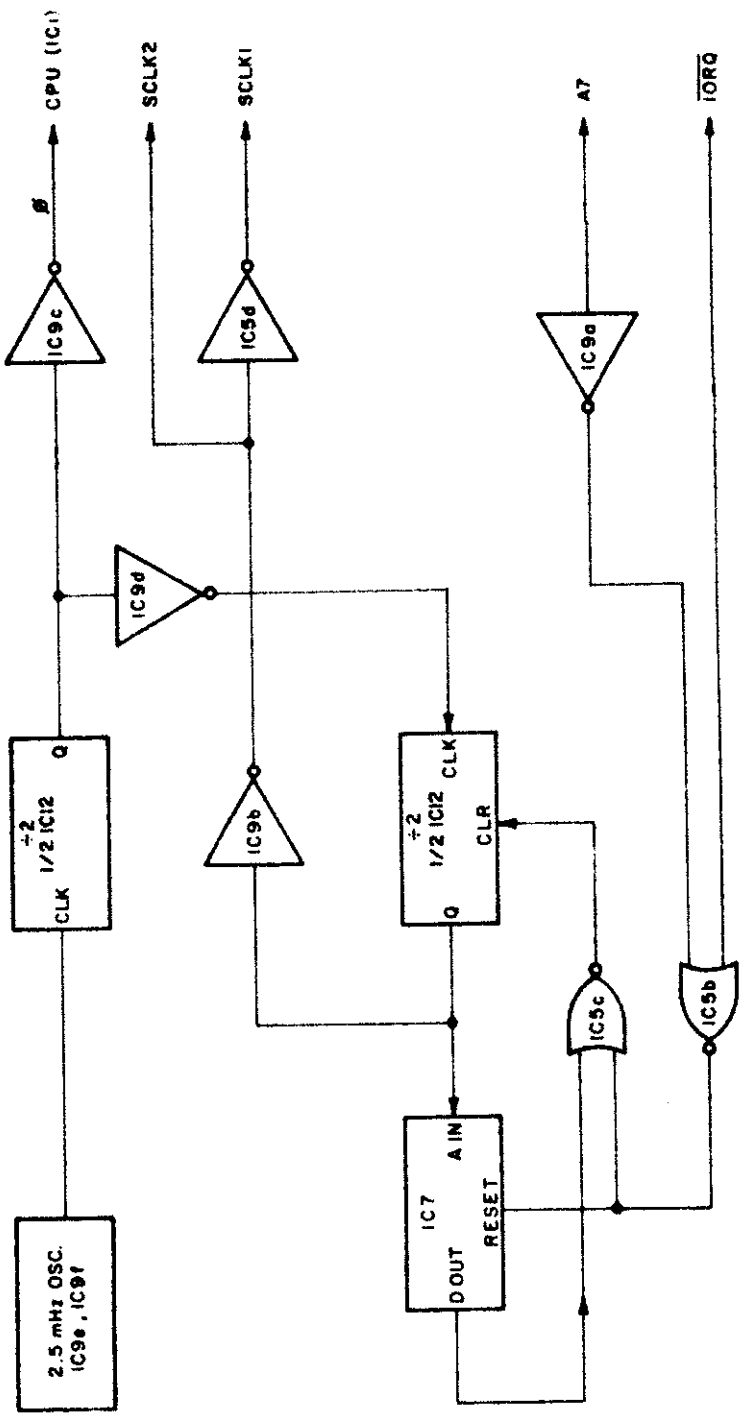


Figure 3-2. Clock and Timing Circuits

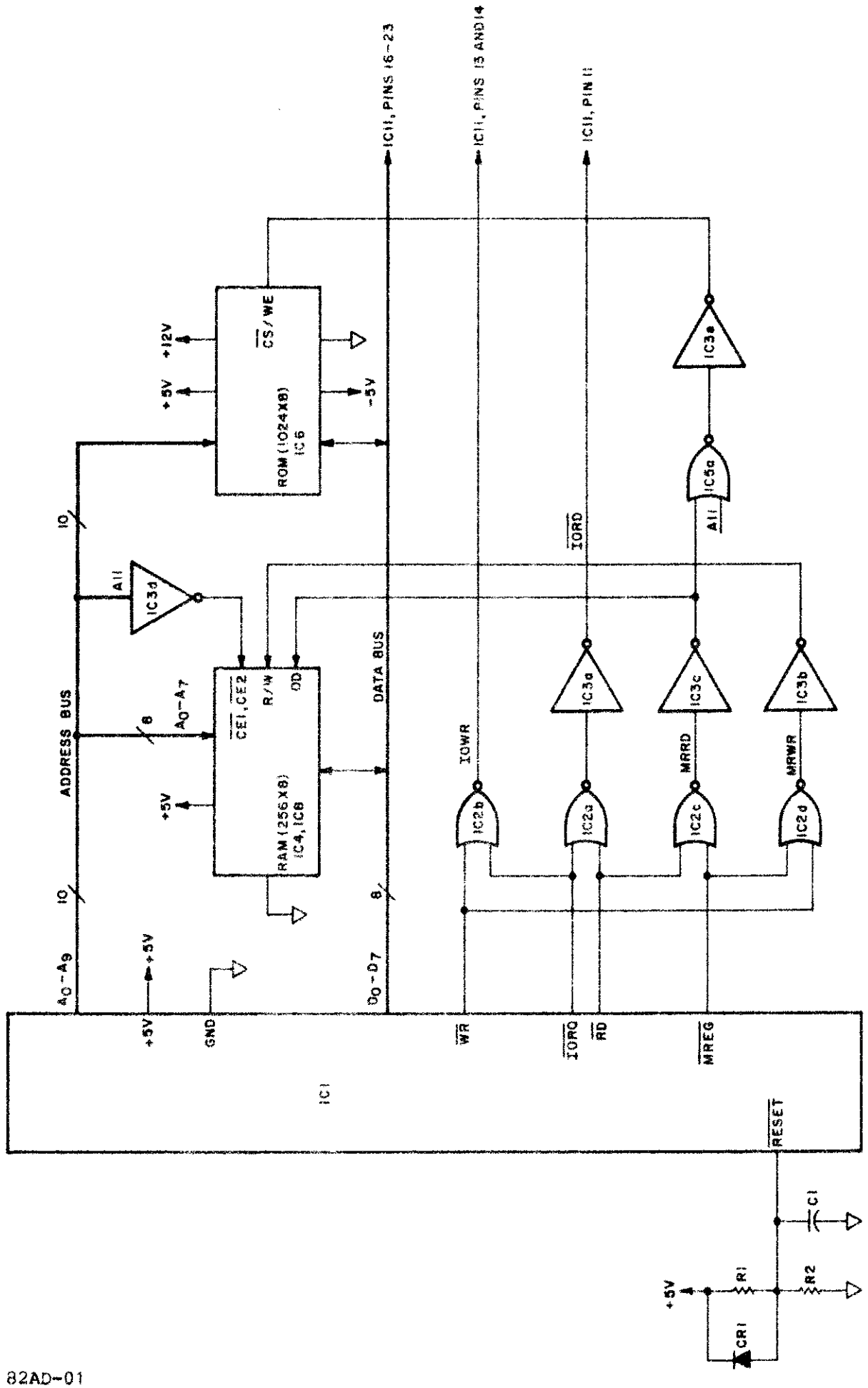
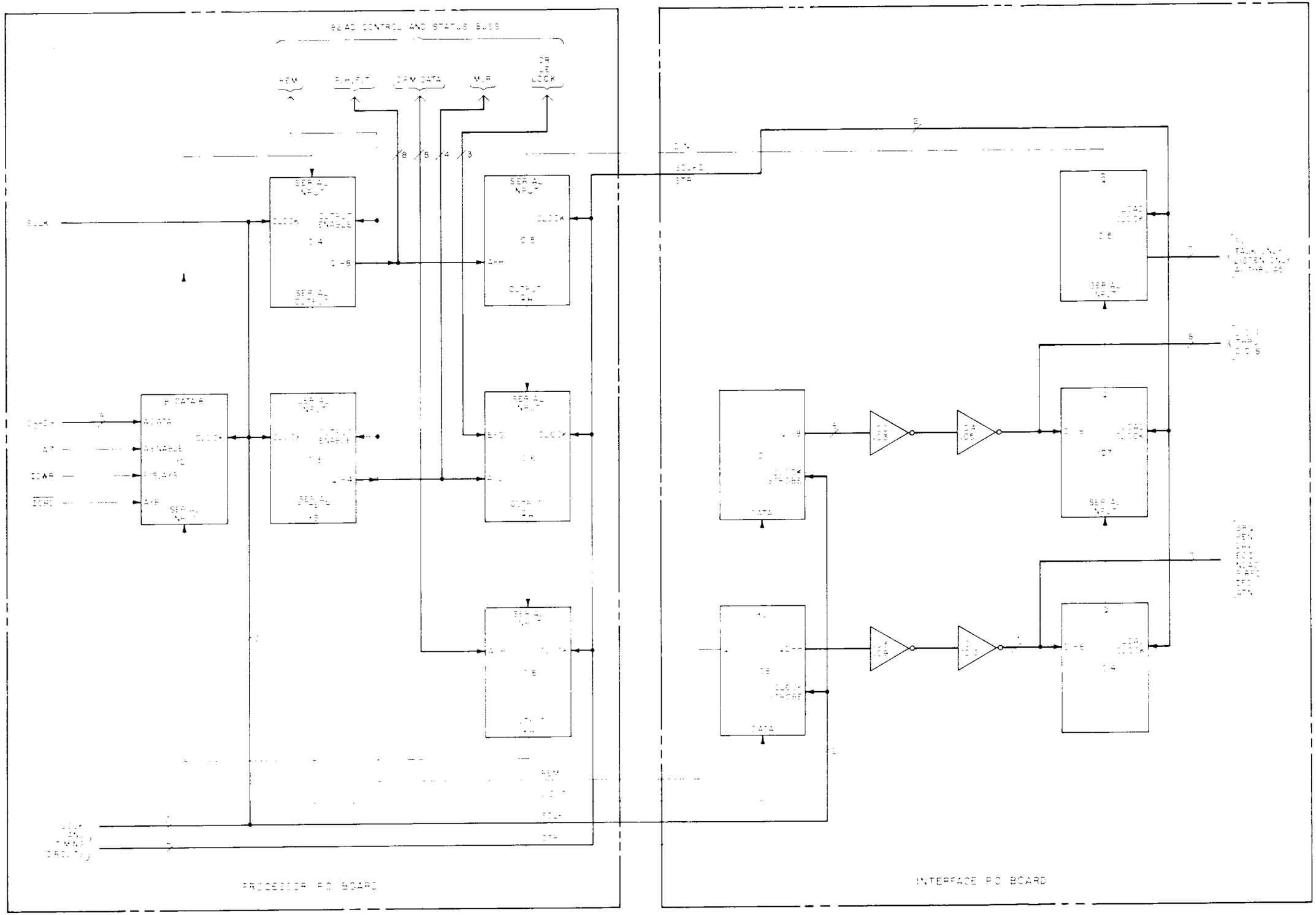


Figure 3-3. CPU and Memory Circuits


READ CONTROL AND STATUS BUSS
REM
R,W,F,T
SERIAL DATA
M,R
OR LE CLOCK
SERIAL INPUT
SERIAL OUTPUT
CLOCK
OUTPUT ENABLE
SERIAL DATA
PROCESSOR P.C. BOARD
INTERFACE P.C. BOARD

3.16 DETAILED THEORY OF OPERATION, SERIAL INTERFACE CIRCUITS. Refer to Figures 3-4, 6-1, and 6-2.

3.17 The digital signals for 488 Bus control, data 82AD control, status and panel meter are all handled by serial input-output ports. On the input side six bytes are required, one each for 488 Data, 488 management plus 82 control line REM1, 82AD status plus "M" and "R" controls lines, 82AD "F", "H", "P", and "T" control lines and 82AD panel meter data. On the output side four bytes are required - one each for 488 Data lines, 488 management, 82AD control lines "M" and "R" and 82AD control lines "F", "H", "P", and "T".

3.18 An input routine consists of an input strobe (address line A15 with I/O write command) followed by a seven byte read sequence. The first byte read is a clear operation for IC11. An output routine consists of a four byte sequential load followed by a data out strobe (address line A14 with an I/O write command).

3.19 IC11 monitors the 8-bit data bus from the Z-80 (IC1) and performs parallel-to-serial and serial-to-parallel conversion for the output ports. In the parallel-in serial-out mode the data appearing on the data bus (DO-07) is loaded and shifted out MSB first followed by the lesser significant bits in descending order. In the serial-in parallel-out mode, data is clocked in MSB first followed by less significant bits in descending order, then parallel output when an I/O read occurs.

SECTION IV

MAINTENANCE

4.1 GENERAL

4.2 This section contains maintenance instructions for the 82AD-01. Included is a list of test equipment required for maintenance and symptomatic trouble-shooting procedures designed to localize a malfunction.

4.3 TEST EQUIPMENT REQUIRED

4.4 Test equipment required for maintenance and adjustment is listed in Table 4-1. Equipment of equivalent characteristics may be substituted for any item listed.

Table 4-1

TEST EQUIPMENT LIST

Item	Nomenclature	Model No.
1	Digital Voltmeter	Data Precision Model 1450
2	Oscilloscope	Hewlett Packard 1740A
3	Logic Probe or Logic Clip	(Optional)

4.5 REMOVING 82AD COVER. Detent handle to top of the cover and remove the four threaded feet on the rear panel. Carefully slide the cover off the 82AD frame.

4.6 PRELIMINARY INSPECTION

4.7 VISUAL CHECK. If equipment malfunction occurs, perform a visual check of the 82AD-01 circuit boards before performing electrical tests. Visual checks

often help to isolate the cause of a malfunction quickly and simply. Inspect the boards for signs of damage caused by excessive shock or vibration, such as: loose hardware; loose electrical connections, and unseated transistors or integrated circuits. Then check for signs of overheating cause by an electrical short circuit. Correct the problems discovered through the visual check. If trouble persists, proceed with electrical checks.

4.8 POWER SUPPLY CHECK. Improper operation of the 82AD-01 may be caused by incorrect operating voltages. Before proceeding with any other electrical checks, perform the power supply checks in accordance with Table 4-2.

Table 4-2

POWER SUPPLY CHECKS

STEP	PROCEDURE	INDICATION	IF INDICATION IS ABNORMAL
1	Remove 82AD cover as outlined above.		
2	Remove tie on the flat cable connecting the processor and interface circuit boards and place the processor board on an extender.		
3	Measure dc voltages at pins 23, 27, and 2 of card edge connector.	Pin — Voltage 23 — +15.0 ±0.02 V 27 — -5 ±0.25 V 2 — +8 to +12 V	Refer to 82AD Manual, Section IV for power supply troubleshooting.
4	Measure voltage at pin 19, IC6.	+12 V nominal	Replace defective Q1 or C4.
5	Measure voltage at pin 24, IC6.	+5 Vdc	Replace defective IC17.

4.9 TROUBLE LOCALIZATION

NOTE: Logical trouble localization involves three major procedures: symptomatic troubleshooting, used to localize the cause of a malfunction to a major circuit group; systematic troubleshooting within the affected circuit group, used to localize the cause of malfunction to a circuit or stage, and voltage and/or waveform measurements, used to isolate the defective part.

4.10 SYMPTOMATIC TROUBLESHOOTING. The modular construction of the 82AD-01 facilitates symptomatic troubleshooting. With a thorough understanding of the detailed block diagrams (Figure 3-1 through Figure 3-4), it is possible to localize the cause of most malfunctions to one or more of the major circuit groups by operating the Bus controller and observing the results. (Refer to Table 4-3.)

4.11 When the cause of an equipment malfunction has been localized to a major circuit group, refer to the appropriate systematic troubleshooting chart (Table 4-4 through Table 4-6). The systematic troubleshooting charts provide instruction for further localization of the cause of the malfunction to a stage or circuit within the major circuit group. When the cause of the malfunction has been localized to a particular stage or circuit, isolate the defective part through voltage and/or waveform measurements. Refer to the schematic diagram for typical voltage and waveform data. (See Figures 6-1 and 6-2.)

4 12 PARTS REMOVAL. Careful attention has been paid in the design of the Model 82AD-01 to maintainability. Most parts are readily accessible for checking and replacement when the case and cover shields are removed. Solid state circuit components are mounted on plug-in printed circuit boards. Standard printed-circuit board maintenance techniques are required for removal and replacement of parts. Excessive heat must be avoided; a low wattage soldering iron and suitable heat sink should be used for all soldering and unsoldering operations.

Table 4-3

SYMPTOMATIC TROUBLESHOOTING CHART

Symptom	Probable Cause of Malfunction
82AD-01 will not "TALK" or "LISTEN".	Defective clock and timing circuits: refer to Table 4-4.
	Defective CPU and memory circuits: refer to Table 4-5.
	Defective serial interface circuits: refer to Table 4-6.
82AD-01 will not "TALK".	Defective serial interface circuits: refer to Table 4-6.
82AD-01 will not "LISTEN".	Defective serial interface circuits; refer to Table 4-6.
	Defective 82AD logic circuits; refer to 82AD Instruction Manual, Section IV.
82AD-01 will not operate in "TALK ONLY" mode.	Defective serial interface circuits: refer to Table 4-6.

Table 4-4. Systematic Troubleshooting Chart

CLOCK AND TIMING CIRCUITS

STEP	PROCEDURE	INDICATION	IF INDICATION IS ABNORMAL
1.	Complete Steps 1 and 2 of Table 4-2 and power on without controller connected.		
2.	Connect an oscilloscope to pin 10, IC9.	Waveform (1), Table 4-7.	Replace defective IC9 or crystal Y1. Check for defective IC12.
3.	Connect oscilloscope to pin 9, IC12.	Waveform (2), Table 4-7.	Replace defective IC12.
4.	Connect oscilloscope to pin 13, IC11.	Waveform (3), Table 4-7.	Defective IC2 or IC11. Defective CPU & memory circuits.
5.	Connect oscilloscope to pin 11, IC11.	Waveform (4), Table 4-7.	Defective IC2, IC3, or IC11. Defective CPU and memory circuits.
6.	Connect oscilloscope to pin 5, IC2.	Waveforms (5) and (6), Table 4-7.	Defective IC12, IC5, IC7.

Table 4-5. Systematic Troubleshooting Chart

CPU AND MEMORY CIRCUITS

STEP	PROCEDURE	INDICATION	IF INDICATION IS ABNORMAL
1.	Complete Table 4-4.		
2.	Check waveform at pin 6, IC1.	Similar to waveform (1), Table 4-7, except flat topped.	Check for defective IC9.
3.	Monitor voltage at pin 26, IC1, with scope and operate power switch off to on and note voltage.	Switch / Voltage OFF 0 Vdc ON +2.5 Vdc	Check for defective C1 or open R1 or shorted CR1.
4.	Check activity on D0 - D7 lines of IC1 (pins 7 - 10, and 12 - 15).	5 volt logic waveform indicating data bus activity.	Replace defective IC1 or IC6, or IC4 and IC8.

Table 4-6. Systematic Troubleshooting Chart

SERIAL INTERFACE CIRCUITS

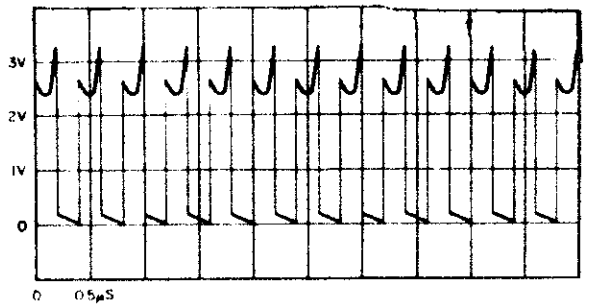
STEP	PROCEDURE	INDICATION	IF INDICATION IS ABNORMAL
1.	Complete Tables 4-4 and 4-5.		
2.	Remove interface board assembly by removing four #4-40 x 1¼" screws holding interface board shield.		
3.	Power on and check for activity at pin 2, IC14.	5 volt logic signal	Replace defective IC11 or IC14.
4.	Check for activity at pin 9, IC14.	5 volt logic signal	Replace defective IC14.
5.	Check for activity at pin 9, IC13.	5 volt logic signal	Replace defective IC13.
6.	Check for activity at pin 9, IC8 on the interface board.	5 volt logic signal	Replace defective IC8.
7.	Check for activity at pin 9, IC1 on the interface board.	5 volt logic signal	Replace defective IC1.
8.	Check for activity at pin 9, IC14 on the interface board.	5 volt logic signal	Replace defective IC14.
9.	Check for activity at pin 9, IC7 on the interface board	5 volt logic signal	Replace defective IC7.

Table 4-6. Systematic Troubleshooting Chart (Continued)

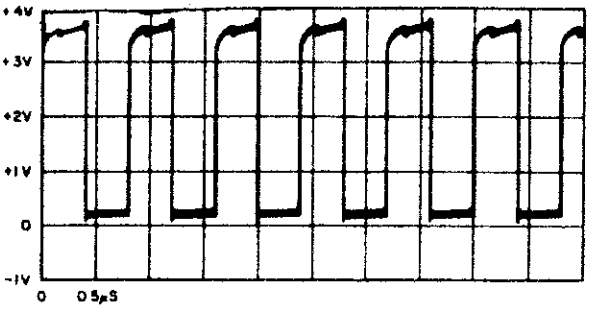
SERIAL INTERFACE CIRCUITS

STEP	PROCEDURE	INDICATION	IF INDICATION IS ABNORMAL
10.	Check for activity at pin 7, IC15 on the processor board.	5 volt logic signal	Replace defective IC15.
11.	Check for activity at pin 9, IC15 on the processor board.	5 volt logic signal	Replace defective IC15.
12.	Check for activity at pin 9, IC16 on the processor board.	5 volt logic signal	Replace defective IC16.
13.	Check for activity at pin 9, IC18 on the processor board.	5 volt logic signal.	Replace defective IC18.
14.	Replace Interface board assembly by replacing four 4-40 x 1-1/4" screws.		

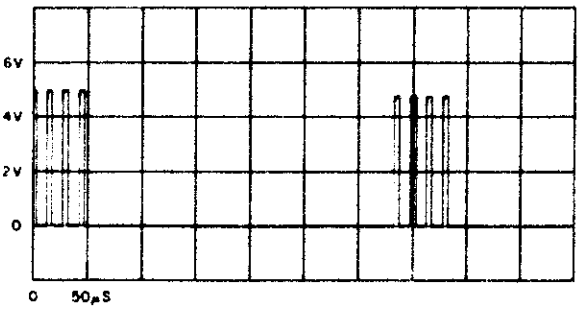
WAVE FORM
PIN 10, IC9



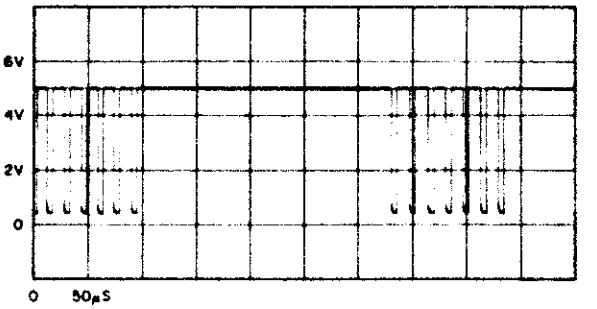
WAVE FORM
PIN 9 IC12



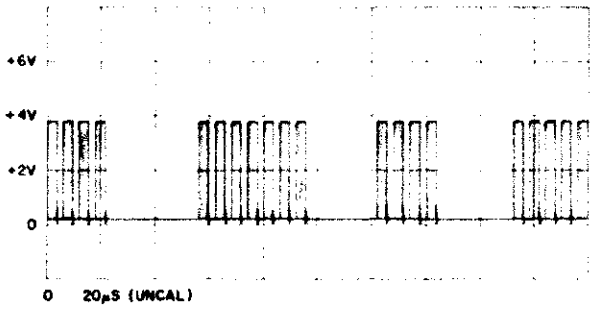
WAVE FORM
PIN 1, IC2



WAVE FORM
PIN 12, IC3



WAVE FORM
PIN 5, IC12



WAVE FORM
PIN 5, IC12

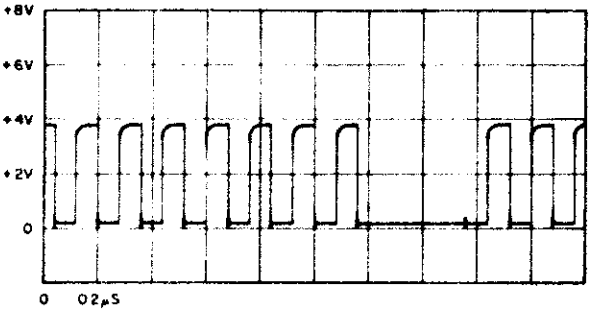


Table 4-7. Waveforms

TABLE OF REPLACEABLE PARTS

Reference	Description		BEC Part No.
	PROCESSOR PC BOARD (A30)		
C1	Capacitor, Tant.	15 µF 10% 20 V	283244
C2	Capacitor, Tant.	10 µF 20% 25 V	283293
C3	Capacitor, Tant.	100 µF 20% 20 V	283313
C4	Capacitor, Tant.	15 µF 10% 20 V	283244
C5	Capacitor, Tant.	10 µF 20% 25 V	283293
CR1	Diode, Sig.	1N914	530058
IC1	Integrated Circuit	Z80 (CPU)	534159
IC2	Integrated Circuit	SN74LS02N (NOR Gate)	534154
IC3	Integrated Circuit	SN74LS04N (Inverter)	534155
IC4	Integrated Circuit	P2111A-4 (RAM)	534162
IC5	Integrated Circuit	SN74LS02N (NOR Gate)	534154
IC6	Integrated Circuit	C2708 (PROM)	534173
IC7	Integrated Circuit	SN74L93N (Counter)	534147
IC8	Integrated Circuit	P2111A-4 (RAM)	534162
IC9	Integrated Circuit	SN7404N (Inverter)	534042
IC10	Integrated Circuit	SN74LS08N (AND Gate)	534156
IC11	Integrated Circuit	CD4034AE (Bus Register)	534158
IC12	Integrated Circuit	SN74LS74N (Flip-Flop)	534157
IC13	Integrated Circuit	CD4094BE (Bus Register)	534149
IC14	Integrated Circuit	CD4094BE (Bus Register)	534149
IC15	Integrated Circuit	MM74C165N (Shift Register)	534160
IC16	Integrated Circuit	MM74C165N (Shift Register)	534160
IC17	Voltage Regulator	µA78MGU1C	535042
IC18	Integrated Circuit	MM74C165N (Shift Register)	534160
L1	Choke	5.6 µH	400308
Q1	Transistor, NPN	2N3642	528128
R1	Resistor, Comp.	22 kΩ 5%	343433
R2 through R5	Resistor, Comp.	1 kΩ 5%	343300
R6	Resistor, Comp.	330 Ω 5%	343250
R7	Resistor, Comp.	470 Ω 5%	343265
R8	Resistor, Comp.	470 Ω 5%	343265
R9	Resistor, MF	6.19 kΩ 1%	341376
R10	Resistor, WW	5 Ω 5% 3 W	312118
R11	Resistor, MF	825 Ω 1%	341288
Y1	Crystal	3.579545 MHz GE 42	547030

Reference	Description			BEC Part No.
	INTERFACE PC BOARD (A31)			
C1	Capacitor, Tant.	33 µF 10% 10 V		283234
IC1	Integrated Circuit	CD4094BE	(Bus Register)	534149
IC2	Integrated Circuit	CD4050AE	(Converter, Non-Inverting)	534092
IC3	Integrated Circuit	CD4050AE	(Converter, Non-Inverting)	534092
IC4	Integrated Circuit	SN7438N	(NAND Buffer)	534108
IC5	Integrated Circuit	SN7438N	(NAND Buffer)	534108
IC6	Resistor Network	3 kΩ/6.2 kΩ 5%		345016
IC7	Integrated Circuit	MM74C165N	(Shift Register)	534160
IC8	Integrated Circuit	CD4094BE	(Bus Register)	534149
IC9	Integrated Circuit	SN74L00N	(NAND Gate)	534002
IC10	Integrated Circuit	SN7404N	(Inverter)	534042
IC11	Integrated Circuit	SN7438N	(NAND Buffer)	534108
IC12	Integrated Circuit	SN7438N	(NAND Buffer)	534108
IC13	Resistor Network	3 kΩ/6.2 kΩ 5%		345016
IC14	Integrated Circuit	MM74C165N	(Shift Register)	534160
IC15	Integrated Circuit	MM74C165N	(Shift Register)	534160
IC16	Resistor Network	3.0 kΩ 2%		345015
J1	Connector	24 Pin	Amph. 57-20240-8	479330
S1	Switch Network		CTS #206-7	465215